IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): An apparatus for transmitting packetized data received from a digital signal processor (DSP) sub-system and host processor in an asynchronous transfer mode (ATM) system, said apparatus comprising:

a first direct memory access unit configured to fetch a voice packet from said DSP sub-system, wherein said voice packet includes a physical phone line identifier; and

a second direct memory access unit configured to fetch a signaling and management packet from said host processor, wherein said signaling and management packet includes a transmit channel identifier.

Claim 2 (Original): The apparatus of Claim 1, wherein said ATM system is an AAL2 module.

Claim 3 (Original): The apparatus of Claim 1 further comprising:

a router identifier table having a memory for storing channel pointers, wherein said physical phone line identifier indexes to a particular channel pointer which identifies a transmit channel in a channel state table; and wherein

said channel state table having a memory for storing channel information for a plurality of transmit channels, said channel information including a pointer to a transmit buffer, wherein said voice and signaling and management packets identified to a particular transmit buffer are forwarded to said particular transmit buffer for further processing and transmission to a destination port.

Claim 4 (Original): The apparatus of Claim 3, wherein a plurality of entries in said router identifier table identifies a particular transmit channel for multiplexing a plurality of physical phone lines onto one ATM channel.

Claim 5 (Original): The apparatus of Claim 3 further including segmentation logic for forwarding voice and signaling and management packet payloads to said particular transmit buffer.

Claim 6 (Original): The apparatus of Claim 1, wherein said first direct memory access unit further operably configured to fetch said voice packet from a voice buffer associated with each digital signal processor in said DSP sub-system.

Claim 7 (Original): The apparatus of Claim 3 implemented in hardware.

Claim 8 (Previously Presented): A system for interleaving voice packets and signaling and management packets on an asynchronous transfer mode (ATM) connection, said system comprising:

a digital signal processor (DSP) system having an input for receiving a voice communication and operably configured to packetize said voice communication and append a corresponding physical phone line identifier;

a host processor operably configured to enable ATM adaptation layer signaling and management and transmit a corresponding signaling and management packet including a transmit channel identifier; and

an ATM transmitter comprising:

a first direct memory access unit configured to fetch a voice packet from said DSP sub-system; and

a second direct memory access unit configured to fetch a signaling and management packet from said host processor.

Claim 9 (Original): The system of Claim 8, wherein said ATM transmitter is implemented in an AAL2 module.

Claim 10 (Original): The system of Claim 8 further comprising:

a router identifier table having a memory for storing channel pointers, wherein said logical channel identifier indexes to a particular channel pointer entry which identifies a transmit channel in a channel state table; and wherein said channel state table having a memory for storing channel information for a plurality of transmit channels, said channel information including a pointer to a transmit buffer, wherein said voice and signaling and management packets identified to a particular transmit buffer for further processing and transmission to a destination port.

Claim 11 (Original): The system of Claim 10, wherein a plurality of entries in said router identifier table identifies a particular transmit channel for multiplexing a plurality of physical phone lines onto one ATM channel.

Claim 12 (Original): The system of Claim 10, wherein said first direct memory access unit further operably configured to fetch said voice packet from a voice buffer associated with each digital signal processor in said DSP sub-system.

Claim 13 (Original): The system of Claim 10, further including segmentation logic for forwarding voice and signaling and management packet payloads to said particular transmit buffer.

Claim 14 (Original): The system of Claim 10 integrated on a silicon chip.

Claim 15 (Original): The system of Claim 10, wherein said ATM transmitter is implemented in hardware.

Claim 16 (Original): A method for transmitting packetized data received from a digital signal processor (DSP) sub-system and a host processor in an asynchronous transfer mode (ATM) system, said method comprising:

fetching a voice packet from said DSP sub-system, said voice packet including a physical phone line identifier corresponding to an originating voice channel supported by said DSP sub-system;

forwarding said voice packet to a transmit buffer associated with a identified transmit channel;

fetching a signaling and management packet from said host processor, said signaling and management packet including a transmit channel identifier; and

forwarding said signaling and management packet to a transmit buffer associated with an identified transmit channel.

Claim 17 (Original): The method of Claim 16, further comprising:

indexing said physical phone line identifier to a set of channel pointers stored in a router identifier table, wherein each of said channel pointers identifies one of a plurality of transmit channel entries in a channel state table; and

indexing said signaling and management packet transmit channel identifier to a transmit channel entry in said channel state table.

Claim 18 (Original): The method of Claim 17 wherein said forwarding voice and signal and management packets comprises forwarding only payloads of each packet.

Claim 19 (Original): The method of Claim 17 further including transmitting data forwarded to said transmit buffer to a destination port associated with said ATM system.

Claim 20 (Original): The method of Claim 17 implemented in hardware.